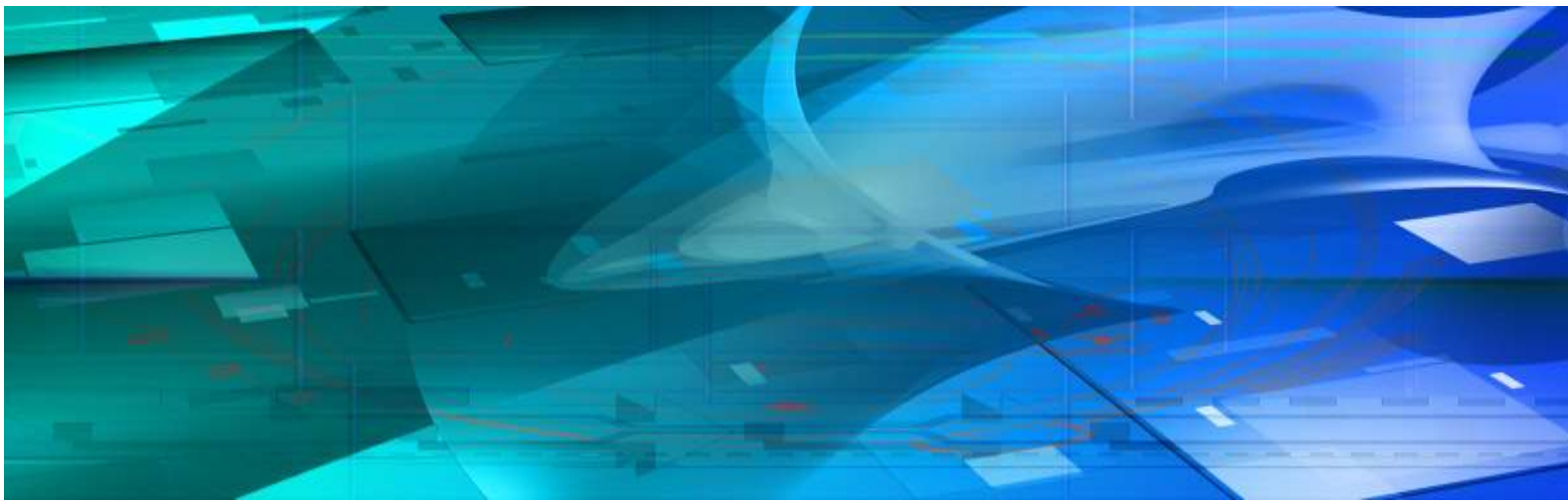
Unigraf DisplayPort™ CTS Tools



Guide to Product Options

UNIGRAF

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Edition

Guide to DP CTS Tool Options, rev 24

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GENERAL

Reference Standards

VESA® DisplayPort® Link Layer Compliance Test Specification Version 1.2 Core Revision 1.1 December 8, 2012

VESA® DisplayPort® Link Layer Compliance Test Specification: Extension Set 1, Rev 1.1, December 28, 2012

HDCP Specification v1.3; Amendment for DisplayPort rev 1.1, 15 Jan 2010

Reduced lane count link training Test Proposal
[James Choate, VESA, 2016-01-20]

Released Versions

This document explains features found in the following versions of the software:

Tool	Version	Issued
Unigraf DP Reference Source CTS	3.3.5	19.08.2015
Unigraf DP Reference Sink CTS	3.3.7	07.11.2014
Unigraf DP LL CTS Ext1 and Core, Set A+B+C+D	1.11	08.06.2016

DP 1.2 LINK CTS

DP Reference Sink Hardware Products

Product	P/N	Description
DPR-120	*065912*	HBR2 and MST compliant Reference Sink

CTS Test Software Product Options for Reference Sinks

Product	P/N	Tests included
Unigraf DP LL CTS Ext1	*065913*	Sets A+B containing link training related tests from DP LL CTS Extensions1 (pls. see lists below)
Unigraf DP LL CTS Ext1 and Core, Set A+B+C	*MC5912*	Sets A+B+C containing link training related tests from DP LL CTS Extensions1 and selected tests from DP LL CTS Core.(pls. see lists below)
Unigraf DP LL CTS Extensions, Upgrade	*065914*	Upgrade from Set A to Sets A+B
DP RefSink LL CTS Upgrade from A+B to A+B+C	*MD5912*	Upgrade from Sets A+B to Sets A+B+C
DP RefSink LL CTS Set D	*MF5912*	Set D (Reduced Lane Count Tests)

Description of CTS Tests for DPR-120

Set A of Link Layer Tests for Testing Transmitter DUT

- DP 1.2 Link Ext1 tests for basic link training functions, HBR2 extension. (Tests 400.3.1.1 to 400.3.1.9)
- Additional DPCD handling tests. (Tests 700.1.1.1, 700.1.1.2)

Test Reference	Test Name
400.3.1.1 (4.3.1.2)	Successful Link Training at All Supported Lane Counts and Link Speeds: HBR2 Extension.
400.3.1.2 (4.3.1.3)	Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence: HBR2 Extension
400.3.1.3 (4.3.1.4)	Successful Link Training to a Lower Link Rate #1: Iterate at Max Voltage Swing: HBR2 Extension
400.3.1.4 (4.3.1.5)	Successful Link Training to a Lower Link Rate #2: Iterate at Minimum Voltage Swing: HBR2 Extension
400.3.1.5 (4.3.1.6)	Successful Link Training with Request of a Higher Pre-emphasis and Post Cursor 2 Setting During Channel Equalization Sequence
400.3.1.6 (4.3.1.7)	Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence: HBR2 Extension
400.3.1.7 (4.3.1.8)	Unsuccessful Link Training at Lower Link Rate #1: Iterate at Max Voltage Swing: HBR2 Extension
400.3.1.8 (4.3.1.9)	Unsuccessful Link Training at Lower Link Rate #2: Iterate at Minimum Voltage Swing: HBR2 Extension
400.3.1.9 (4.3.1.10)	Unsuccessful Link Training due to Failure in Channel Equalization Sequence (loop count > 5): HBR2 Extension
700.1.1.1 (7.1.1.1)	Additional DPCD Handling Test 1
700.1.1.2 (7.1.1.2)	Additional DPCD Handling Test 2

In column Test Reference, the test in (parenthesis) indicates the corresponding test in DP 1.2 Link Core.

Set B of Link Layer Tests for Testing Transmitter DUT

- DP 1.2 Link Ext1 tests for link configuration changes, HBR2 extension.
  (Tests 400.3.1.12 to 400.3.1.15; 400.3.2.1 to 400.3.2.3)
- Video stamp generation (Test 400.3.3.1)

In column Test Reference, the test in parenthesis indicates the corresponding test in DP 1.2 Link Core.

Test Reference	Test Name
400.3.1.12	Successful Link Training to a Lower Link Rate #3: Iterate at Max Voltage Swing
400.3.1.13	Successful Link Training to a Lower Link Rate #4: Iterate at Minimum Voltage Swing
400.3.1.14	Successful Link Downgrade to Lowest Link Rate: Failed Clock Recovery at HBR2, Loss of Clock Recovery during Channel Equalization at HBR
400.3.1.15	Successful Link Training with Simultaneous Request for Differential Voltage Swing and Post Cursor during Clock Recovery & Channel Equalization Sequences
400.3.2.1 (4.3.2.1)	Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol Lock: HBR2 Extension
400.3.2.2 (4.3.2.2)	Successful Link Re-training After IRQ HPD Pulse Due to Loss of Clock Recovery Lock: HBR2 Extension
400.3.2.3 (4.3.2.3)	Successful Link Re-training After IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock: HBR2 Extension
400.3.3.1 (4.3.3.1)	Video Time Stamp Generation

In column Test Reference, the test in (parenthesis) indicates the corresponding test in DP 1.2 Link Core.

Set C of Link Layer Tests for Testing Transmitter DUT

- Partial set of tests from DP 1.2 CTS Core not covered by Ext1.

Test Reference	Test Name
4.2.1.1	Source DUT Retry on No-Reply During AUX Read after HPD Plug Event
4.2.1.2	Source Retry on Invalid Reply During AUX Read after HPD Plug Event
4.2.2.1	EDID Read upon HPD Plug Event
4.2.2.2	DPCD Receiver Capability Read upon HPD Plug Event
4.2.2.3	EDID Read
4.2.2.4	EDID Read Failure #1: I2C-Over-AUX NACK
4.2.2.5	EDID Read Failure #2: I2C-Over-AUX DEFER
4.2.2.6	EDID Corruption Detection
4.2.2.7	Branch Device Detection upon HPD Plug Event
4.2.2.8	EDID Read on IRQ HPD Event after Branch Device Detection
4.2.2.9	E-DDC Four Block EDID Read
4.3.2.4	Handling of IRQ HPD Pulse with No Error Status Bits Set
4.3.2.5	Lane Count Reduction
4.3.2.6	Lane Count Increase
4.4.1.1	Data Packing and Steering
4.4.1.2	Main Stream Data Packing and Stuffing - Least Packed TU
4.4.1.3	Main Stream Data Packing and Stuffing - Most Packed TU
4.4.2	Main Video Stream Format Change Handling
4.4.3	Power Management

In column Test Reference, the test in (parenthesis) indicates the corresponding test in DP 1.2 Link Core.

Set D of Link Layer Tests for Testing Transmitter DUT

- Reduced lane count link training Test Proposal
  [James Choate, VESA, 2016-01-20]
- This test confirms that the Source DUT follows the fallback requirements in case of only lane 0 or Lane 0/1 available due to channel limitation, DP Alt Mode configuration or using active USB-C to USB-C cable.

Test Reference	Test Name
Test1	CR failure on Lane2/3
Test2	CR failure on Lane1/2/3
Test3	Symbol Lock failure on Lane2/3
Test4	Symbol Lock failure on Lane1/2/3

DP 1.1 REFSINK CTS TOOLS

DP Reference Sink Hardware Products

Product	P/N	Description
DPR-100	*065910*	Compact sized DP 1.1 compliant Reference Sink with DP Sink Console software

CTS Test Software Product Options for Reference Sinks

Product	P/N	Tests included
DP RefSink HDCP CTS	*065035*	- HDCP CTS for Testing Transmitters
DP RefSink Extended HDCP CTS Upgrade	*065039*	- Extended HDCP CTS for testing Transmitters and Repeaters
DP RefSink Audio CTS	*065043*	- Audio CTS for Testing Transmitters

Description of CTS Tests for Reference Sinks

HDCP CTS for Testing Transmitter DUT

Test Reference	Test Name
(1A-01)	Regular Procedure: With Receiver
(1A-02)	Regular Procedure: HPD After Writing Aksv
(1A-03)	Regular Procedure: HPD During Link Integrity Check Stage
(1A-04)	Irregular Procedure: (First Part of Authentication) Failure to Read Bcaps HDCP_CAPABLE Bit
(1A-05)	Irregular Procedure: (First Part of Authentication) Verify Bksv
(1A-06)	Irregular Procedure: (First Part of Authentication) Verify R0'
(1A-07)	Irregular Procedure: (Link Integrity Check) Link Integrity Failure
(1A-08)	Irregular Procedure: SRM
(1A-09)	Regular Procedure: Encryption Disable Bootstrapping

Extended HDCP CTS for Testing Transmitter and Repeater DUT

Tests for Transmitter DUT:

Test Reference	Test Name
(1B-01)	Regular Procedure: With Repeater
(1B-02)	Irregular Procedure: Spurious CP_IRQ Interrupt
(1B-03)	Regular Procedure: HPD after Reading R0'
(1B-04)	Irregular Procedure: (Second part of Authentication) Timeout of KSV List READY
(1B-05)	Irregular Procedure: (Second part of Authentication) Verify V'
(1B-06)	Irregular Procedure: (Second part of Authentication) MAX_DEVS_EXCEEDED
(1B-07)	Irregular Procedure: (Second part of Authentication) MAX_CASCADE_EXCEEDED

Tests for Repeater DUT:

Test Reference	Test Name
(3A-01)	Regular Procedure: With Receiver
(3A-02)	Irregular Procedure: (First part of Authentication) Failure to Read Bcaps HDCP_CAPABLE Bit
(3A-03)	Irregular Procedure: (First part of Authentication) Verify Bksv
(3A-04)	Irregular Procedure: (First part of Authentication) Verify R0'
(3B-01)	Regular Procedure: With Repeater
(3B-02)	Irregular Procedure: (Second part of Authentication) Timeout of KSV List READY
(3B-03)	Irregular Procedure: (Second part of Authentication) Verify V'
(3B-04)	Irregular Procedure: (Second part of Authentication) MAX_DEVS_EXCEEDED
(3B-05)	Irregular Procedure: (Second part of Authentication) MAX_CASCADE_EXCEEDED

Audio CTS for Testing Transmitter DUT

Test Reference	Test Name
(4.4.4.2)	Audio Stream Header Synchronization *(Note: Always Skipped, HW does not support the test procedure)*
(4.4.4.3)	Audio Time Stamp Generation
(4.4.4.4)	Audio InfoFrame Packet
(4.4.4.5)	Audio Stream Transmission
(4.4.4.6)	Audio Start Sequence

DP 1.1 REFSOURCE CTS TOOLS

Reference Source and Sink Hardware Products

Product	**P/N**	**Description**
DPT-200	065921	Compact sized DP 1.1 compliant Reference Source with DP Source Console software
VTG-5225 DP	065031	DP 1.1 compliant Reference Source and Pattern Generator with WinVTG GUI software
DPR-100	*065910*	DPR-100 Reference Sink can be used as Pseudo Sink or Pseudo Repeater in HDCP CTS. *Please contact Unigraf for details.*

CTS Test Software Product Options for Reference Sources

Product	**P/N**	**Tests included**
DP RefSource CTS LL	065032	- Link Layer CTS for testing Receivers
DP RefSource CTS LL & HDCP	065036	- Link Layer CTS for testing Receivers - HDCP CTS for Testing Receivers
DP RefSource CTS LL & HDCP & EXT HDCP	065045	- Link Layer CTS for testing Receivers - HDCP CTS for Testing Receivers - Extended HDCP CTS for Testing Repeaters

Description of CTS Tests for Reference Sources

Link Layer CTS for testing Receiver DUT

Test Reference	Test Name
(5.2.1.1)	Read One Byte from Valid DPCD Address
(5.2.1.2)	DPCD Receiver Capability Read (Read Twelve Bytes from Valid DPCD Address)
(5.2.1.3)	Write One Byte to Valid DPCD Address
(5.2.1.4)	Write Nine Bytes to Valid DPCD Addresses
(5.2.1.5)	Write EDID Offset (One Byte I2C-Over-Aux Write)
(5.2.1.6)	Read One EDID Byte (One Byte I2C-Over-Aux Read)
(5.2.1.7)	EDID Read (1 Byte I2C-Over-Aux Segment Write, 1 Byte I2C-Over-Aux Offset Write, 128 Byte I2C-Over-Aux Read)
(5.2.1.8)	Illegal Aux Request Syntax
(5.2.1.9)	Glitch Rejection

Link Layer CTS for testing Receiver DUT (cont.d)

(5.2.1.10)	Interleaved EDID and DPCD Receiver Capability Read
(5.2.1.11)	Downstream Stop on MOT Reset
(5.2.1.12)	Downstream Stop on MOT Timeout
(5.3.1.1)	Successful Link Training at All Supported Lane Counts and Link Speeds
(5.3.1.2)	Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence
(5.3.1.3)	Successful Link Training to a Lower Link Rate Due To Clock Recovery Lock Failure During Clock Recovery Sequence
(5.3.1.4)	Successful Link Training with Request of a Change to Pre-Emphasis and/or Voltage Swing Setting During Channel Equalization Sequence
(5.3.1.5)	Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence
(5.3.1.6)	Lane Count Reduction
(5.3.1.7)	Lane Count Increase
(5.3.2.1)	IRQ_HPD Pulse Due to Loss of Symbol Lock and Clock Recovery Lock
(5.3.2.2)	IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock
(5.4.1.1)	Pixel Data Reconstruction
(5.4.1.2)	Main Stream Data Unpacking and Unstuffing – Least Packed TU
(5.4.1.3)	Main Stream Data Unpacking and Unstuffing – Most Packed TU
(5.4.1.4)	Pixel Clock Recovery *(Note: Informative, HW does not support SSC)*
(5.4.2)	Main Video Stream Format Change Handling
(5.4.3.1)	Entering and Exiting Power Save Mode
(5.4.3.2)	Resumption of Main Link Activity After Extended Idle
(7.2.1.1)	Sink Organizationally Unique Identifier (OUI)
(7.2.1.2)	Sink Count
(7.2.1.3)	Sink Status
(7.2.1.4)	Symbol Error Count
(7.2.1.5)	Device Identifications
(7.2.1.6)	Number of Receiver Ports
(7.2.1.7)	Main Link Channel Coding

HDCP CTS for Testing Receiver DUT

Test Reference	Test Name
(2A-01)	Regular Procedure: With Transmitter
(2A-02)	Irregular Procedure: (First Part of Authentication) New Authentication
(2A-03)	Irregular Procedure: (Link Integrity Check) New Authentication
(2A-04)	Regular Procedure: Encryption Disable Bootstrapping

Extended HDCP CTS for Testing Repeater DUT

Test Reference	**Test Name**
(3C-01)	Regular Procedure: Transmitter - DUT - Receiver
(3C-02)	Regular Procedure: HPD Propagation when an Active Receiver is Disconnected and Reconnected Downstream
(3C-03)	Regular Procedure: HPD Propagation when an Active Receiver is Disconnected Downstream
(3C-04)	Regular Procedure: HPD Propagation when an Active Receiver is Connected Downstream
(3C-05)	Irregular Procedure: (First part of Authentication) New Authentication
(3C-06)	Irregular Procedure: (Second part of Authentication) New Authentication
(3C-07)	Irregular Procedure: (Link Integrity Check) New Authentication
(3C-08)	Irregular Procedure: (Second part of Authentication) Verify Bksv
(3C-09)	Irregular Procedure: (Second part of Authentication) Verify R0'
(3C-10)	Regular Procedure: Transmitter - DUT - Repeater
(3C-11)	Regular Procedure: HPD After Writing Aksv
(3C-12)	Regular Procedure: HPD After Reading R0'
(3C-13)	Regular Procedure: HPD After Starting Third part of Authentication
(3C-14)	Irregular Procedure: (Second part of Authentication) Verify V'
(3C-15)	Irregular Procedure: (Second part of Authentication) DEVICE_COUNT
(3C-16)	Irregular Procedure: (Second part of Authentication) DEPTH
(3C-17)	Irregular Procedure: (Second part of Authentication) MAX_DEVS_EXCEEDED
(3C-18)	Irregular Procedure: (Second part of Authentication) MAX_CASCADE_EXCEEDED

Note	Please contact Unigraf for details on using DPR-100 Reference Sink as Pseudo Sink or Pseudo Repeater in HDCP CTS.

Audio CTS for Testing Receiver DUT

Currently not available